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BEFORE THE BOARD OF PATENT APPEALS

AND INTERFERENCES

Paper No. 22

Application Number: 09/476,862

Filing Date: 1-3-00

Appellant(s): Tsukihashi

John P. Scherlacher

For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed on 7-23-03.

(1) Real Party in Interest

A statement identifying the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

A statement identifying the related appeals and interference which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

(3) Status of Claims

The statement of the status of the claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Invention

The summary of invention contained in the brief is correct.

(6) Issues

The appellant's statement of the issues in the brief is correct.

(7) Grouping of Claims

The rejection of claims 3-12 stand or fall together because appellant's brief does not include a statement that this grouping of claims does not stand or fall together and reasons in support thereof. See 37 CFR 1.192(c)(7).

(8) Claims Appealed

The copy of the appealed claims contained in the Appendix to the brief is correct.

(9) Prior Art of Record

The following is a listing of the prior art of record relied upon in the rejection of claims under appeal.

5,436,875	Shinada	7-1995
5,434,997	Landry et al.	7-1995

(10) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 U.S.C. § 103

1. The following is a quotation of 35 U.S.C. § 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
>
> Subject matter developed by another person, which qualifies as prior art only under subsection (f) or (g) of section 102 of this title, shall not preclude patentability under this section where the subject matter and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person.

2. Claims 3-12 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Shinada et al., US. patent 5,436,875 (hereafter Shinada) in view of Landry et al., US. patent 5,434,997 (hereafter Landry).

As to claim 3, Shinada discloses the invention as claimed [see Figs. 1-16] including a buffer memory, a data processing circuit and a system control circuit, a write circuit comprising:

As to claim 3, Shinada discloses::

a. a buffer memory fig. 1, units 18 and 22] for temporarily storing the received data [col. 6, lines 1-5];

b. a data processing circuit [fig. 1, units 14 and 6] for preparing the recording data to record onto the disk [col. 3, line 61 to col. 4, line 2], based on the received data read from the buffer memory [col. 6, lines 54-59; and

c. a system control circuit [fig. 1, unit 10] for controlling writing and reading of the received data with respect to the buffer memory, and operation of the data processing circuit [col. 5, lines 40-42 and col. 5, lines 65-68], and

d. A writing circuit [fig.1, unit 4] for writing the recorded data supplied from the data processing circuit onto the disk [col. 5, lines 18-39];

e. wherein the system control circuit [fig. 1, unit 10] suspends operation of the data processing circuit until an amount of received data equivalent to a predetermined writing capacity [memory 22 drops below the fixed volume or not; col. 8, lines 34-35] has been stored in the buffer memory, and releases suspension of the operation of the data processing circuit when an amount of received data equivalent to the predetermined writing capacity has been stored in the buffer memory [col. 8, lines 19-55];

f. wherein the system control circuit stores an address successive to an address of received data last recorded [position information] onto the disk [data previously stored], as a recording start address on the disk, and controls the writing circuit so as to write the recording data supplied from the data processing circuit onto the disk as the recording start address [col. 1, lines 51-57; col. 5, lines 51-64 and col. 12, lines 48-68]; and

g. wherein the system control circuit synchronizes the recording data to be newly recorded onto the disk, supplied from the data processing circuit to the writing circuit, with recording data

recorded on the disk [col. 6, lines 12-28], said data processing circuit being operated in synchronism with a reproduction clock obtained by reproducing the data already recorded on the disk [col. 2, lines 14-17; col. 7, line 38 to col. 8, line 30; col. 9, lines 15-29].
NOTE: When processing steps are repeated, the head is returned to the previous reproducing position [col. 8, lines 19-26]. This step inherently has to synchronize the recording data to be newly recorded data, so as to start from the same spot where the old data has stopped recording.

Shinada discloses all of the above elements including system control circuit for suspending the operation of the data processing circuit [col. 8, lines 19-30]. Shinada does not specifically disclose how his system is suspending this operation and details of the suspension circuit and data being placed in a suspended state by interrupting the power supply or by halting an operation clock to the extent claimed. However Landry clearly discloses:

the data processing circuit for recording data being placed in a suspended state by interrupting the power supply or by halting the supply of an operation clock [col. 2, lines 19-40 and col. 16, lines 13-61; Landry]. Both Shinada and Landry are interested in controlling the recording operation of the data and avoiding wrong data recording by checking the data content against some reference point [such as threshold or fixed volume of data] and controlling the recording operation. Also both are aware that most of the data processing systems are interrupt driven and need to store data in the buffer because of interrupts that inherently arises from time to time. It would have been obvious to one of ordinary skill in the at the time of invention to have provided the system of Shinada with details of controlling the data recording by halting the system clock as disclosed by Landry, because doing so would have provided a mechanism for localizing an error or fault on the spot and easily correct it [see col. 1, lines 13-30; Landry], in order to implement the suggested invention of Shinada.
NOTE: Shinada clearly discloses that his invention can be practiced on, THREE kind of optical discs [col. 3, lines 59-60], including ROM [that is Read Only Memory, which is by definition a non-erasable, write-once {when it was originally written} memory], RAM [read and write] and hybrid [some areas are ROM and some areas are RAM] [see col. 3, line 61 to col. 4, line 2].

3. As to claim 4, Shinada discloses:

. a motor control circuit [fig. 1, unit 7] for controlling a motor for driving the disk, wherein the motor control circuit controls the motor such that the disk rotates, while operation of the data processing circuit is suspended at a same speed as that at which the disk rotated immediately before the suspension of data recording [col. 5, lines 3-30 and col. 6, lines 35-40];
NOTE: Shinada discloses that disc rotates under constant linear velocity [col. 5, lines 5-6]. Shinada also discloses that disc is able to start the recording function again without stopping the inputting the data signal S1. In other words the disc speed is constant before and after the suspension of the recording.

4. As to claim 5 Shinada does not specifically discloses that the buffer memory is set at a full memory capacity. "Official Notice" is taken that both the concept and the advantages of setting the buffer memory capacity at full capacity are well known in the art. It would have been obvious to provide a full capacity to buffer memory in Shinada's system as this setting the capacity to full allows the system to use the full capability of the buffer. Since real estate in the integrated circuits and on the board are at premium one of ordinary skill in the art would have been able to provide the mechanism to use full capability of the buffer so as not to waste premium space in the buffer. These concepts are well known in the art and do not constitute a patentably distinct limitation, per se [M.P.E.P. 2144.03].

5. As to claim 6, Shinada discloses:

the writing capacity of the buffer memory is set at the capacity of the buffer memory deducted by an amount of data expected to be written into the buffer memory before data recording onto the disk is resumed [col. 6, lines 16-27].

Shinada discloses all of the above elements. Shinada does not specifically discloses that the buffer memory is set at a full memory capacity. "Official Notice" is taken that both the concept and the advantages of setting the buffer memory capacity at full capacity are well known in the art. It would have been obvious to provide a full capacity to buffer memory in Shinada's system as this setting the capacity to full allows the system to use the full capability of the buffer. Since real estate in the integrated circuits and on the board are at premium one of ordinary skill in the art

would have been able to provide the mechanism to use full capability of the buffer so as not to waste premium space in the buffer. These concepts are well known in the art and do not constitute a patentably distinct limitation, per se [M.P.E.P. 2144.03].
NOTE: recording or writing stops when the memory capacity minus expected data limit is reached. In other words memory 18 data falls below a prescribed value or threshold.

6. As to claim 7, Shinada discloses:

a. a buffer memory fig. 1, units 18 and 22] for temporarily storing the received data [col. 6, lines 1-5];

b. a data processing circuit [fig. 1, units 14 and 6] for preparing the recording data to record onto the disk, based on the received data read from the buffer memory [col. 6, lines 54-59; and

c. a system control circuit [fig. 1, unit 10] for controlling writing and reading of the received data with respect to the buffer memory, and operation of the data processing circuit [col. 5, lines 40-42 and col. 5, lines 65-68]; and

d. a writing circuit [fig. 1, unit 4] for writing the recorded data supplied from the data processing circuit, onto the disk, wherein the system control circuit suspends operation of the data processing circuit until an amount of received data equivalent to a predetermined writing capacity has been stored in the buffer memory, and releases suspension of the operation of the data processing circuit to resume writing of the recording data onto the disk by the writing circuit when an amount of received data equivalent to the predetermined writing capacity has been stored in the buffer memory [col. 8, lines 19-55].

Shinada discloses all of the above elements including system control circuit for suspending the operation of the data processing circuit [col. 8, lines 19-30]. Shinada does not specifically disclose how his system is suspending this operation and details of the suspension circuit and data being placed in a suspended state by interrupting the power supply or by halting an operation clock to the extent claimed. However Landry clearly discloses:

the data processing circuit for recording data being placed in a suspended state by interrupting the power supply or by halting the supply of an operation clock [col. 2, lines 19-40 and col. 16, lines 13-61; Landry]. Both Shinada and Landry are interested in controlling the recording

operation of the data and avoiding wrong data recording by checking the data content against some reference point [such as threshold or fixed volume of data] and controlling the recording operation. Also both are aware the most of the data processing system are interrupt driven and need to store data in the buffer because of interrupts. It would have been obvious to one of ordinary skill in the at the time of invention to have provided the system of Shinada with details of controlling the data recording by halting the system clock as disclosed by Landry, because doing so would have provided a mechanism for localizing an error or fault on the spot and easily correct it [see col. 1, lines 13-30; Landry], in order to implement the suggested invention of Shinada.

7. As to claim 8, Shinada discloses:

the system control circuit stores an address successive to an address of received data last recorded [position information] onto the disk [data previously stored], as a recording start address on the disk, and controls the writing circuit so as to write the recording data supplied from the data processing circuit onto the disk as the recording start address [col. 1, lines 51-57; col. 5, lines 51-64 and col. 12, lines 48-68].

8. As to claim 9, Shinada discloses:

wherein the system control circuit synchronizes the recording data to be newly recorded onto the disk, supplied from the data processing circuit to the writing circuit, with recording data recorded on the disk , said data processing circuit being operated in synchronism [simultaneously] with a reproduction clock obtained by reproducing the data already recorded on the disk [col. 2, lines 14-17; col. 7, lines 38-52; col. 9, lines 15-29].

9. As to claim 10, Shinada discloses:

a motor control circuit [fig. 1, unit 7] for controlling a motor for driving the disk, wherein the motor control circuit controls the motor such that the disk rotates, while operation of the data processing circuit is suspended at a same speed as that at which the disk rotated immediately before the suspension of data recording [col. 5, lines 3-30 and col. 6, lines 35-40];

NOTE: Shinada discloses that disc rotates under constant linear velocity [col. 5, lines 5-6]. Shinada also discloses that disc is able to start the recording function again without stopping the inputting the data signal S1. In other words the disc speed is constant before and after the suspension of the recording.

10. As to claim 11 Shinada does not specifically discloses that the buffer memory is set at a full memory capacity. "Official Notice" is taken that both the concept and the advantages of setting the buffer memory capacity at full capacity are well known in the art. It would have been obvious to provide a full capacity to buffer memory in Shinada's system as this setting the capacity to full allows the system to use the full capability of the buffer. Since real estate in the integrated circuits and on the board are at premium one of ordinary skill in the art would have been able to provide the mechanism to use full capability of the buffer so as not to waste premium space in the buffer. These concepts are well known in the art and do not constitute a patentably distinct limitation, per se [M.P.E.P. 2144.03].

11. As to claim 12, Shinada discloses:

the writing capacity of the buffer memory is set at full memory capacity of the buffer memory deducted by an amount of data expected to be written into the buffer memory before data recording onto the disk is resumed [col. 6, lines 16-27].

NOTE: recording or writing stops when full memory capacity minus expected data limit is reached. In other words memory 18 data falls below a prescribed value or threshold.

(11) Response to Argument

In the REMARKS, the Applicant argues as follows:

A) That: "it is stated in the Final Office Action that the ROM (read-only-memory) referred to in Shinada includes a "write-once" media. However, the disc of Shinada is a CD (compact disc) which is used for reproduction only. Nowhere does Shinada disclose that such disc is writable." [page 4, para. 2; REMARKS]; and

"The reproduction-only disk (of Shinada) is a music CD in which no writing is performed. With the description "reproduction-only" being used in the specification, it is very clear that the disk (of Shinada) is not a CD-R." [page 4, para. 3; REMARKS; explanatory parenthetical phrase added].

FIRST: Appellant is referring to the preamble limitation in claim 3 regarding the disk being "non-erasable, write-once". It is noted that independent claim 7 does NOT recite this feature and all claims stand or fall together.

SECOND: Shinada clearly discloses that "This invention relates to an optical disc device, and more particularly, to a magneto-optical disc device which **records and**/or **reproduces** the desired data on the disc shaped recording medium .." [col. 1, lines 11-15; Shinada]

THIRD: Shinada also clearly discloses that his invention can be practiced on **three kinds** of optical discs [col. 3, lines 59-60]. In other words RAM, ROM and combination thereof.

B) That: "Moreover, Shinada does not disclose or suggest generating a reproduction clock and operating in synchronization with such clock. [page 4, para. 5; REMARKS].

FIRST: Appellant is referring to the limitation in claim 3, last 3 lines, that the "data processing circuit being operated in synchronism with a reproduction clock". It is noted that independent claim 7 does NOT recite this feature at all and all claims stand or fall together.

SECOND: Shinada does not use word synchronization, but Shinada does disclose this aspect as can be clearly seen from rejection and explanation above. Also word simultaneously exactly describes the aspect of synchronism in Shinada patent [col. 2, lines 14-17], because something can not be done simultaneously unless two events are synchronized to happen at the same time. As a matter of fact Shinada patent depends on this aspect of simultaneous reproduction and recording.

C) That: "The present invention differs from Landry. In the case of the present invention, operation is suspended by interrupting the power supply **or** [emphasis added] **halting the supply of an operation clock** when buffer underrun occurs." [page 4, para. 5; REMARKS].

Landry discloses: "a mirror error is generated, which halts the system clock [= operation clock]. This effectively halts the entire system, ..", [col. 2, lines 31-40]. Mirror error is based on writing data in the buffer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Gautam R. Patel

August 9, 2003

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